CRE	Datasheet	No.	DS10-QR003
		Initial Date	2024-02-28
OQR	OQRC3D102	Written Team	R&D Dept. GH Zheng

I Preview

PN	OQRC3D102
Description	800G QSFP-DD 2xFR4 1310nm-CWDM 2KM dual duplex LC DDMI 0~70 °C

II Contents

III Revision History

No.	Date	Items	Change Recording	Ver.	Rev.	Customer
1	2024-02-28	All	Initial registration	000	000	Standard
2						
3						
4						
5						
6						

1. Features

- Compliant with QSFP-DD800 MSA HW Rev 6.01 with dual duplex LC connector
- Compliant with IEEE 802.3cu-2021:
  - 2x400GBASE-FR4 optical interface
- Compliant with IEEE P802.3ck D3.0
  - 2x400GAUI-4 C2M electrical interface
- Compliant with CMIS Rev 5.0
- Two wire serial Interface with digital diagnostic monitoring
- RoHS compliant
- Operating case temperature: Standard: 0 to +70°C

2. Applications

- 8x100G Ethernet
- 2x400G Ethernet
- Other links

3. Description

The OCRECOM's OQRC3D102 is a module is designed for use in 800 Gigabit Ethernet links over 2km single mode fiber. The module has 8 independent electrical input/output channels operating up to 106.25Gbps per channel. This transceiver consists of two transmitter/receiver units, with each operating on a set of 4 wavelengths on the ITU G.694.2 CWDM grid near 1300nm.

4. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	TST	-40	85	℃	
Relative Humidity(non-condensing)	RH	5	85	%	
Operating Case Temperature	TOPC	0	70	℃	
Supply Voltage	VCC	-0.5	3.6	V	
Data Input Voltage Differential	$\lvert V_{DP}-V_{DN}\rvert$	-	1	V	
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V	
Control Output Current	I_o	-20	20	mA	

5. Operating Environment

Parameter	Symbol	Min	Typical	Max	Unit	Note
Operating Case Temperature	TOPC	0		70	℃	

Power Supply Voltage	VCC	3.13	3.3	3.47	V	
Instantaneous peak current at hot plug	I_{CC_P}	-	-	6800	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	5611	mA	
Power dissipation		-		17	W	
Power dissipation, Low Power Mode		-		2	W	
Signalling Speed per Lane	DRL		53.125		Gbd	
Control Input Voltage High	V_{IH}	V_{CC}*0.7	-	V_{CC}+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3	-	V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance		2		2000	m	

6. Optical Characteristics

All parameters are specified under the recommended operating conditions with PRBS31 data pattern unless otherwise specified.

Transmitter						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Wavelength L0, L4	$\lambda_{C0}, \lambda_{C4}$	1264.5	1271	1277.5	nm	
Wavelength L1, L5	$\lambda_{C1}, \lambda_{C5}$	1284.5	1291	1297.5	nm	
Wavelength L2, L6	$\lambda_{C2}, \lambda_{C6}$	1304.5	1311	1317.5	nm	
Wavelength L3, L7	$\lambda_{C3}, \lambda_{C7}$	1324.5	1331	1337.5	nm	
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P_T			10.4	dBm	
Average Launch Power, each lane	P_{AVG}	-3.2	-	+4.4	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane for TDECQ <1.4 dB for 1.4 dB ≤TDECQ ≤3.4 dB	T_{OMA}	-0.2 –1.6 + TDECQ	-	3.7	dBm	
Difference in launch power between any two lanes (OMAouter)	AOP_d	-	-	3.9	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	

Transmitter eye closure for PAM4 (TECQ), each lane	TECQ	-	-	3.4	dB	
|TDECQ – TECQ|	-	-	-	2.5	dB	
Over/under-shoot	-	-	-	22	%	
Transmitter power excursion	-	-	-	1.8	dBm	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-16	dBm	
Extinction Ratio	ER	3.5	-	-	dB	
Transmitter transition time (max)	Tr	-	-	17	ps	
RIN$_{21}$OMA (max)	RIN	-	-	-136	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	17.1	dB	
Transmitter Reflectance	T_R			-26	dB	2
Average Launch Power OFF Transmitter, each Lane	P_{off}			-20	dBm	

Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Wavelength L0, L4	λ_{C0}, λ_{C4}	1264.5	1271	1277.5	nm	
Wavelength L1, L5	λ_{C1}, λ_{C5}	1284.5	1291	1297.5	nm	
Wavelength L2, L6	λ_{C2}, λ_{C6}	1304.5	1311	1317.5	nm	
Wavelength L3, L7	λ_{C3}, λ_{C7}	1324.5	1331	1337.5	nm	
Damage Threshold	THd	5.4			dBm	
Average Receive Power, each Lane	AOP_R	-7.2		4.4	dBm	
Receive Power (OMA), each Lane	OMA_R			3.7	dBm	
Receiver sensitivity (OMAouter), each lane for TECQ < 1.4 dB for 1.4 dB≤ TECQ ≤3.4 dB	SOMA			-4.6 –6 + TECQ	dBm	
Stressed Receiver Sensitivity (OMA), each Lane	SRS			-2.6	dBm	3
Receiver Reflectance	R_R			-26	dB	
Difference in Receive Power between any Two Lanes (OMA)	AOP_g			4.1	dB	
Conditions of Stress Receiver Sensitivity Test						
Stressed eye closure for PAM4 (SECQ), lane under test	-	-	3.4	-	dB	

OMAouter of each aggressor lane	-	-	1.4	-	dBm	

Notes:

1, Average launch power, each lane (min) is informative and not the principal indicator of signal strength

2, Transmitter reflectance is defined looking into the transmitter

3, Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$

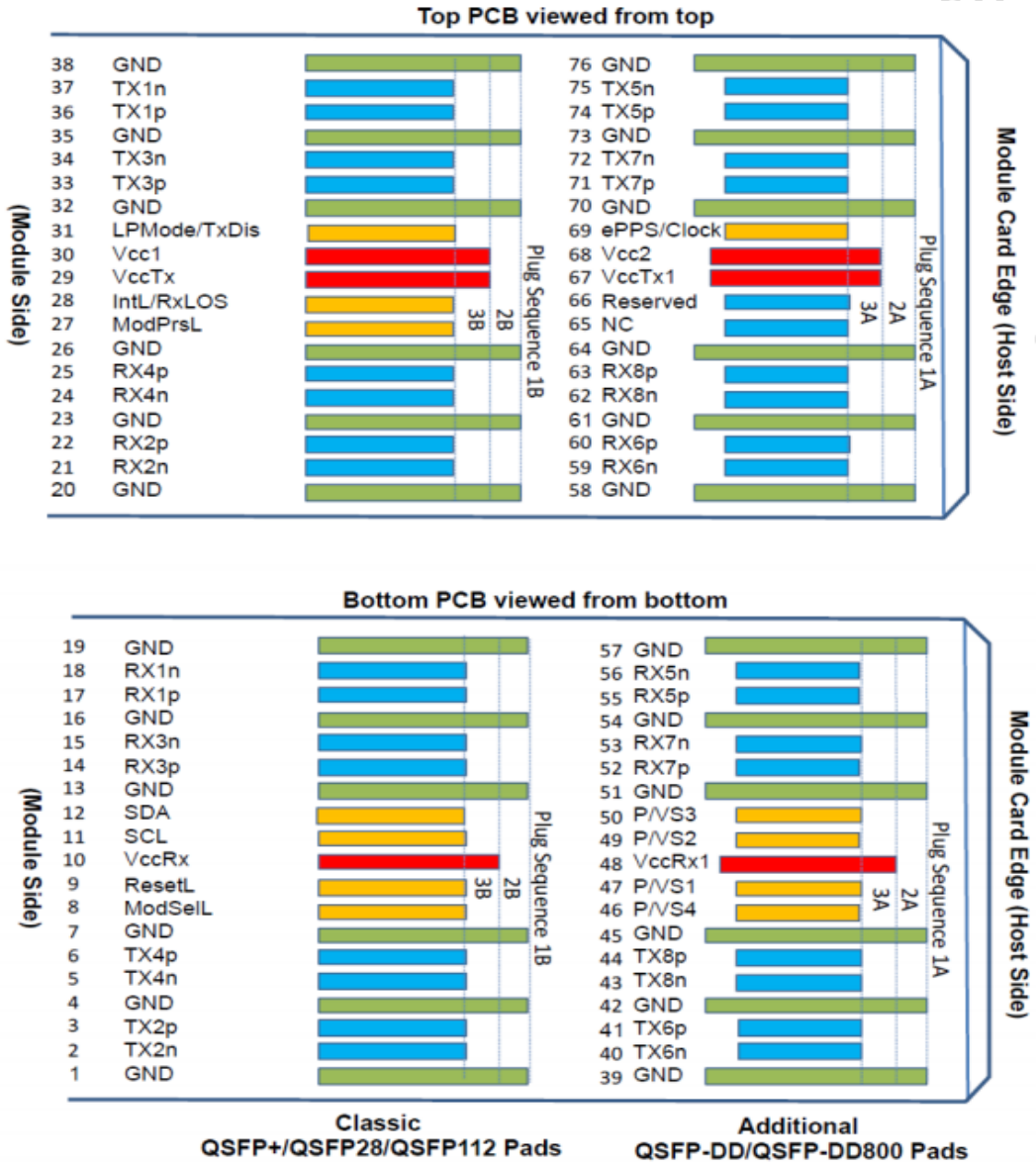
7. Electrical Specifications

Transmitter (Module Input, TP1)						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Units**	**Notes**
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	mV	
AC common-mode RMS voltage tolerance (TP1a)	-	25	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
Receiver (Module Output, TP4)						
AC common-mode output Voltage (RMS)	-	-	-	25	mV	
Differential peak-to-peak output voltage Short mode Long mode	-	-	-	 600 845	mV	
Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Transition time	-	8.5	-	-	ps	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
Electrical Specification Low Speed Control and Sense Signals						
Module output SCL and SDA	V_{OL}	0		0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3		Vcc*0.3	V	

	V_{IH}	Vcc*0.7		Vcc+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3		0.8	V	
	V_{IH}	2		Vcc+0.3	V	
IntL	V_{OL}	0		0.4	V	
	V_{OH}	Vcc-0.5		Vcc+0.3	V	

8. Pin Descriptions

The electrical pinout of the QSFP-DD module is shown in below.



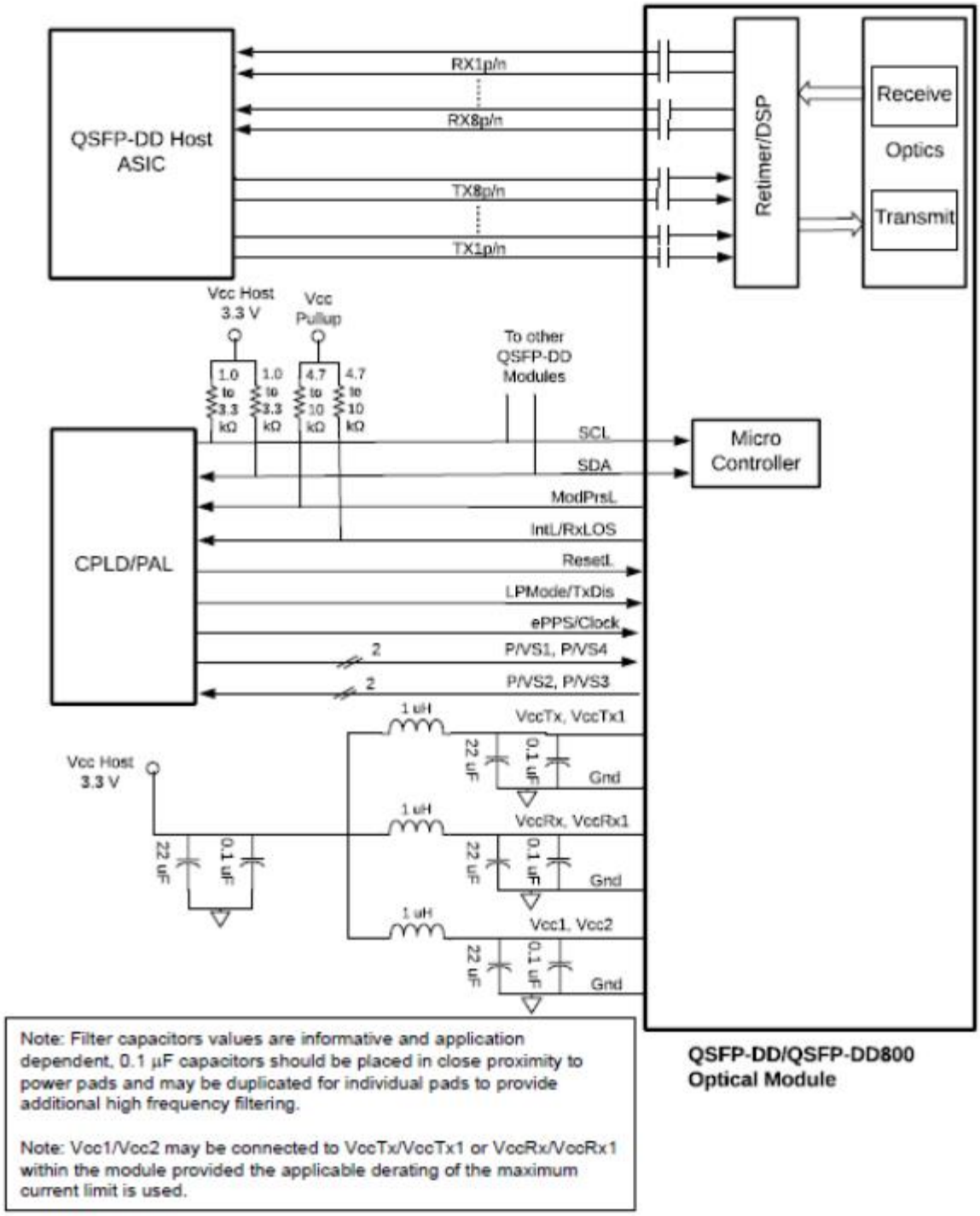
MSA Compliant Connector

PIN	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	TWI serial interface clock
12	LVCMOS-I/O	SDA	TWI serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLoss
29		VccTx	+3.3V Power supply transmitter
30		Vcc1	+3.3V Power supply
31	LVTTL-I	LPMode/Tx Dis	LPMODE/optional Tx Disable

32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45		GND	Ground
46	LVCMOS/CML I	P/VS4	Programmable/Module Vendor Specific 4
47	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1
48		VccRx1	3.3V Power Supply
49	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2
50	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61		GND	Ground

62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64		GND	Ground
65		NC	No Connect
66		Reserved	For future use
67		VccTx1	3.3V Power Supply
68		Vcc2	3.3V Power Supply
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

Recommended QSFP-DD/QSFP-DD800 Host Board Schematic



Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

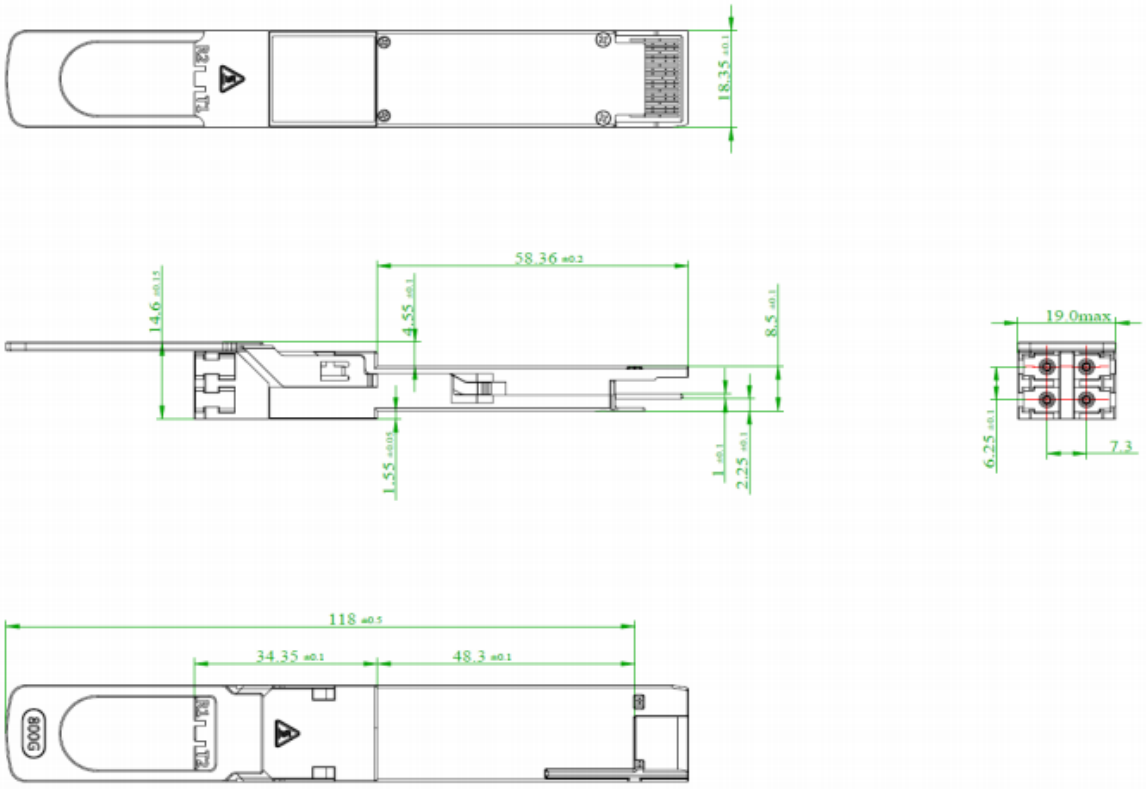
Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

9. Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Unit	Notes
Temperature monitor absolute error(0~70 ˚C)	DMI_Temp	-3	+3	degC	Over operating temp
Supply voltage monitor absolute error (3.13~3.47V)	DMI_VCC	-0.1	0.1	V	Full operating range
Channel RX power monitor absolute error (-7.2~+4.4dB)	DMI_RX	-3	3	dB	Per channel
Channel Bias current monitor (0~100mA)	DMI_Ibias	-10%	10%	mA	Per channel
Channel TX power monitor absolute error (-3.2~+4.4dB)	DMI_TX	-3	3	dB	Per channel

10. Mechanical Dimensions



11. Module Ordering information

PN	Description
OQRC3D102	2x400G QSFP-DD FR4 1300nm-CWDM 2KM dual duplex LC DDMI 0~70 ˚C