CRE	Datasheet	No.	DS10-L021
		Initial Date	2024-08-19
OL	OLQDC41Z	Written Team	R&D Dept.
			GH Zheng

I Preview

PN	OLQDC41Z
Description	400G CFP2-DCO Module

II Contents

III Revision History

No.	Date	Items	Change Recording	Ver.	Rev.	Customer
1	2024-02-22	All	Initial registration	000	000	Standard
2	2024-08-19	All	Special customer	001	000	Special
3						
4						
5						
6						

1. Features

The module of OLQDC41Z is CFP2 form coherent pluggable module compliant to the CFP MSA CFP2 Hardware Specification, based on DP-mQAM modulation, polarization diversity coherent Intradyne detection and advanced electronic link equalization. On the host side, the module can accommodate a variety of signal types including 4x100GE, 2x 200GE, 1x 400GE, OTUCn(n=[1..4]), and OTU4. On the line side, the module supports 100G, 200G, 300G, and 400G interfaces with different modulation formats and forward error correction (FEC) codes. Multiple 100G clients can be multiplexed onto a single 200G, 300G, or 400G line side interface. The module support LLDP function.

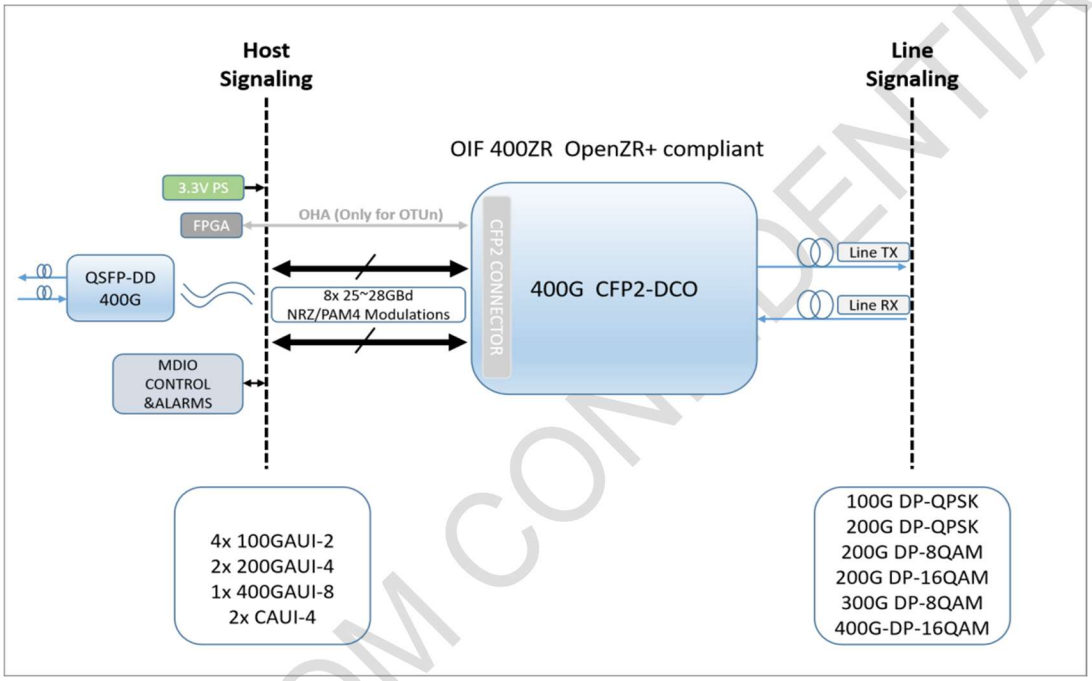

Figure 1 Module function diagram

The module of OLQDC41Z is a complete implementation of a high-performance coherent transceiver capable of operating in high performance telecom and datacenter.

2. Applications

The module of OLQDC41Z operates as an Ethernet/OTN transceiver/transponder or a Muxceiver/MuxPonder aggregates up to 2x200G and 4×100GE modes at the Host/Client interface up to its configured line-side optical capacity.

Table 1 Line-side Mode

Media Lane Interface	Line	FEC	Framing	Symbol Rate(Gbaud)
100G 100ZR-OFEC-QPSK	100G QPSK	OFEC	100ZR+	30.07
100G FOIC1-OFEC-QPSK	100G QPSK	OFEC	FLEXO-1	31.57
200G 200ZR-OFEC-QPSK	200G QPSK	OFEC	200ZR+	60.14

200G 200ZR-OFEC-8QAM	200G 8QAM	OFEC	200ZR+	40.09
200G 200ZR-OFEC-16QAM	200G 16QAM	OFEC	200ZR+	30.07
200G FOIC2-OFEC-QPSK	200G QPSK	OFEC	FLEXO-2	63.14
200G FOIC2-OFEC-8QAM	200G 8QAM	OFEC	FLEXO-2	42.09
200G FOIC2-OFEC-16QAM	200G 16QAM	OFEC	FLEXO-2	31.57
300G 300ZR-OFEC-8QAM	300G 8QAM	OFEC	300ZR+	60.14
300G FOIC3-OFEC-8QAM	300G 8QAM	OFEC	FLEXO-3	63.14
400G 400ZR-CFEC-16QAM	400G 16QAM	CFEC	400ZR	59.84
400G 400ZR-OFEC-16QAM	400G 16QAM	OFEC	400ZR+	60.14
400G FOIC4-OFEC-16QAM	400G 16QAM	OFEC	FLEXO-4	63.14

Table 2 Host-side Mode

Protocol	Interface	FEC	Signaling and termination	Rate(Gbaud) per lane	Reference Standards
Ethernet	4×100GAUI-2	RS-FEC(544,514)	PAM-4 Signaling, internally terminated, and AC couple	26.5625 (+/-100ppm)	IEEE 802.3TM-2018 Clause 91, 119 Annex 120E (C2M)
	1x400GAUI-8				
	2 x 200GAUI-4				
	2×CAUI-4	NONE	NRZ Signaling, internally terminated, and AC coupled	25.78125 (+/-100ppm)	IEEE 802.3TM-2018, Clause 83D, 93, 91, and Annex 83E(C2M)
	2×CAUI-4 w/FEC	RS-FEC(528,514)			
OTUCn (n=[1..4])	1 x FOIC4.8-RS	RS-FEC (544,514)	PAM-4 Signaling, internally terminated, and AC coupled	27.952369 (+/-20ppm)	ITU-T G.709.1 Y.133.1 ITU-T G.Sup58 (10/2018) IEEE 802.3TM-2018 Clause 91, 119 Annex 120E (C2M) OIF-CEI-04.0 CEI-56G-VSR-PAM4 Very Short Reach Interface - Clause 16
	2 x FOIC2.4-RS				
	4 x FOIC1.2-RS				
	2x OTLC.4	GFEC (255,239)	NRZ Signaling, internally terminated, and AC coupled	28.076177 (+/-20ppm)	ITU-T G.Sup58 (10/2018) OIF-CEI-04.0 CEI-28G-VSR Very Short Reach Interface - Clause 13
OTU4	2x OTL4.4	GFEC (255,239)	NRZ Signaling, internally terminated, and AC coupled	27.952493 (+/-20ppm)	

	4x OTL4.2	GFEC (255,239)	PAM-4 Signaling, internally terminated, and AC coupled		

3. Description

The OCRECOM's OLQDC41Z is a coherent optical module uses a 104-pin connector as an electrical interface to connect the system board. The module comprises TX unit, RX unit and control units. All control interface pins work properly with the help of the internal MCU which itself can also be used for modulator control, software management, alarm performance reporting and other functions.

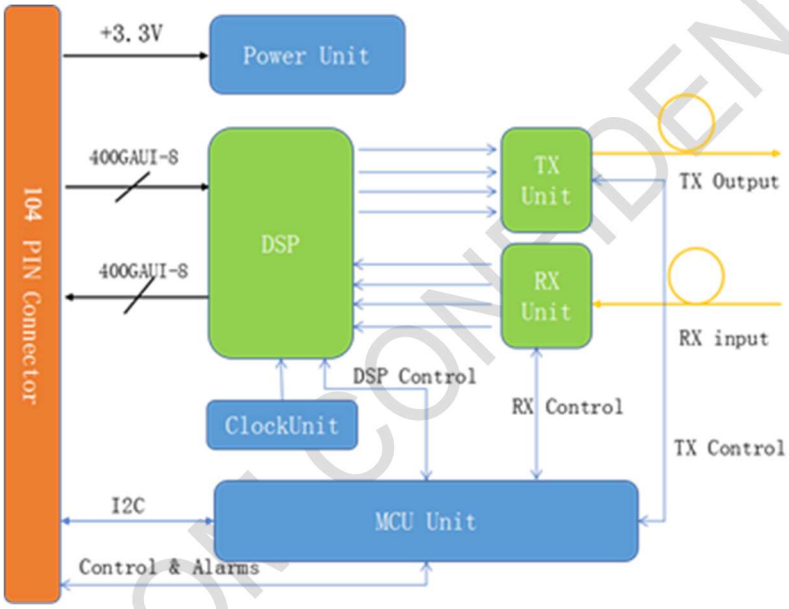

Figure 2 Module Block Diagram

4. Operating Environment

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Table 3 Operation Environment

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	TST	-40	85	℃	
Relative Humidity(non-condensing)	RH	5	85	%	
Operating Case Temperature	TOPC	0	70	℃	
Power Supply	VCC	3.135	3.465	V	
Operating Power Consumption			25	w	
Power Consumption			2.75	w	LP mode

5. OPTIC AND ELECTRIC SPECIFICATION

Table 4 Specification

Parameter	Measurement Conditions	Min	Typ	Max	Unit
Transmitter					
Baud Rate	Per IQ modulator	27.95		64	Gbaud
Modulation Formats		DP-16QAM/DP-8QAM/DP-QPSK			
Mean modulated output power		-10	0	+3	dBm
Shuttered output power	Total output power with Tx disabled			-35	dBm
Wavelength range		1528.578		1567.337	nm
Frequency range		191.3		196.1	THz
Default Channel grid spacing	Tunable across C-band	6.25	75	100	GHz
Channel grid spacing	Adjustable over C-band	0.1			GHz
Frequency accuracy		-1.5		1.5	GHz
Frequency fine tune range	Fine tuning with Tx output enabled (bright tuning)	-6		6	GHz
Lorentzian linewidth	Tx and LO			300	kHz
Tx output power monitor accuracy	Tx optical output power monitor reading relative to actual Tx output power (-15~+3dBm)	-1.5		1.5	dB
OSNR	Inband	38			dB
OSNR	Outband	33			dB
Optical transmitter turn on time	Warm start			6	s
Optical transmitter turn on time	Cold start			116	s
Optical transmitter turn off time	From Tx_DIS assert			10	ms

Transmitter channel tuning time	Channel to channel			86	s
Optical return loss	towards the module	27			dB

Receiver					
Input Power range	100G 100ZR-OFEC-QPSK	-32		1	dBm
	100G FOIC1-OFEC-QPSK	-32			
	200G 200ZR-OFEC-QPSK	-29			
	200G 200ZR-OFEC-8QAM	-28			
	200G 200ZR-OFEC-16QAM	-24			
	200G FOIC2-OFEC-QPSK	-28			
	200G FOIC2-OFEC-8QAM	-28			
	200G FOIC2-OFEC-16QAM	-23			
	300G 300ZR-OFEC-8QAM	-23			
	300G FOIC3-OFEC-8QAM	-23			
	400G 400ZR-CFEC-16QAM	-20			
	400G 400ZR-OFEC-16QAM	-21			
	400G FOIC4-OFEC-16QAM	-20			
VOA range	On input signal	10			dB
VOA step size				0.1	dB
VOA response time				100	ms
Signal input monitor accuracy	-22dBm～+3dBm	-1.8		1.8	dB
OSNR Sensitivity (Standard range)	400G FOIC4-OFEC-16QAM		22	23.5	dB
	400G 400ZR-OFEC-16QAM		22	23	
	400G 400ZR-CFEC-16QAM			26	
	300G FOIC3-OFEC-8QAM			20.5	
	300G 300ZR-OFEC-8QAM			20.3	

	200G FOIC2-OFEC-16QAM			20	
	200G FOIC2-OFEC-8QAM			17.5	
	200G FOIC2-OFEC-QPSK			15.7	
	200G 200ZR-OFEC-16QAM			19.3	
	200G 200ZR-OFEC-8QAM			17.2	
	200G 200ZR-OFEC-QPSK			14.8	
	100G FOIC1-OFEC-QPSK			11.8	
	100G 100ZR-OFEC-QPSK			11.5	
Chromatic Dispersion tolerance OSNR Oebaktt<0.5dB	400G FOIC4-OFEC-16QAM	24			ns/nm
	400G 400ZR-OFEC-16QAM	26			
	400G 400ZR-CFEC-16QAM	2.4			
	300G FOIC3-OFEC-8QAM	48			
	300G 300ZR-OFEC-8QAM	50			
	200G FOIC2-OFEC-16QAM	25			
	200G FOIC2-OFEC-8QAM	48			
	200G FOIC2-OFEC-QPSK	48			
	200G 200ZR-OFEC-16QAM	30			
	200G 200ZR-OFEC-8QAM	50			
	200G 200ZR-OFEC-QPSK	50			
	100G FOIC1-OFEC-QPSK	77			
	100G-100ZR-OFEC-QPSK	80			
SOP Tolerance OSNR Oebaktt<0.5dB	400G FOIC4-OFEC-16QAM	80			Krad/s
	400G 400ZR-OFEC-16QAM	80			
	400G 400ZR-CFEC-16QAM	50			
	300G FOIC3-OFEC-8QAM	120			
	300G 300ZR-OFEC-8QAM	100			
	200G FOIC2-OFEC-16QAM	50			

	200G FOIC2-OFEC-8QAM	70			
	200G FOIC2-OFEC-QPSK	800			
	200G 200ZR-OFEC-16QAM	50			
	200G 200ZR-OFEC-8QAM	70			
	200G 200ZR-OFEC-QPSK	800			
	100G FOIC1-OFEC-QPSK	400			
	100G 100ZR-OFEC-QPSK	400			
PDL tolerance (peak)	Tolerance to peak PDL with < 1.3 dB penalty to OSNR sensitivity when change in SOP is <=1 rad/ms.			3.5	dB
Optical return loss		20			dB
Rx total input power	The Rx total input power of all channels.			13	dBm

6. Pin Descriptions

The electrical pinout of the CFP2 module is shown in Figure 3 below.

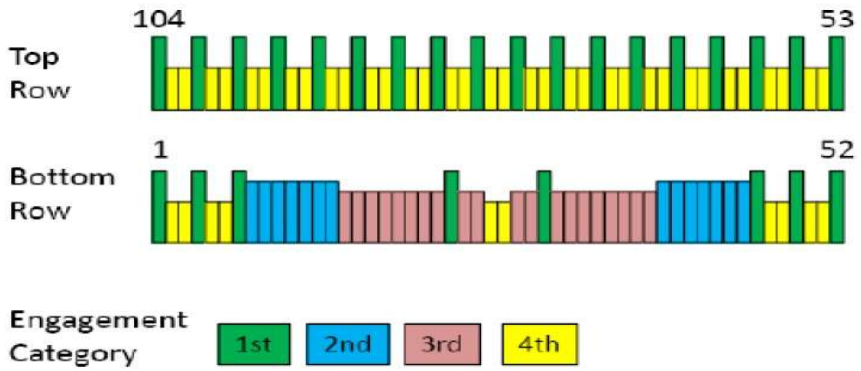

Figure 3 PIN assignment

Table 5 MSA Compliant Connector

PIN	Name	I/O	Logic	Description
1	GND	GND	Ground	Module Ground. Logic and power return path
2	OHIO_RDn	O	CML	

3	OHIO_RDp	O	CML	OHIO Drop interface; Interface is differentially AC coupled, internal to module.
4	GND	GND	Ground	Module Ground. Logic and power return path
5	OHIO_TDn	I	CML	OHIO Insert interface; Interface is differentially AC coupled, terminated, and biased internal to module.
6	OHIO_TDp	I	CML	
7	3.3V_GND	PWR_GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
8	3.3V_GND	PWR_GND	Ground	
9	3.3V	PWR	Power	3.3V power supply input
10	3.3V	PWR	Power	
11	3.3V	PWR	Power	
12	3.3V	PWR	Power	
13	3.3V_GND	PWR_GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
14	3.3V_GND	PWR_GND	Ground	
15	NC			
16	NC			
17	PRG_CNTL1	I	3.3V LVCMOS	Internal 4.7k pull-up; TRXIC_RSTn, TX & RX IC reset. “0”: reset.
18	PRG_CNTL2	I	3.3V LVCMOS	Internal 4.7k pull-up; Hardware Interlock LSB
19	PRG_CNTL3	I	3.3V LVCMOS	internal 4.7k pull-up; Hardware Interlock MSB
20	PRG_ALRM1	O	3.3V LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up
21	PRG_ALRM2	O	3.3V LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready, Internally Pull-Up
22	PRG_ALRM3	O	3.3V LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
23	GND	GND	Ground	Module Ground. Logic and power return path
24	TX_DIS	I	3.3V LVCMOS	Transmitter Disable, Internally Pull-Up
25	RX_LOS	O	3.3V LVCMOS	Receiver Loss of Signal
26		I	3.3V	Module Low Power Mode, Internally Pull-Up

	MOD_LOPWR		LVCMOS	
27	MOD_ABS	O	3.3V LVCMOS	Module Absent, Internally Pull-Down
28	MOD_RSTn	I	3.3V LVCMOS	Module Reset, Active Low, Internally Pull-Down
29	GLB_ALRMn	O	3.3V LVCMOS	Global Alarm, Active Low
30	GND	GND	Ground	Module Ground. Logic and power return path
31	MDC	I	1.2V LVCMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
32	MDIO	I/O	1.2V LVCMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	PRTADR0	I	1.2V LVCMOS	MDIO Physical Port address bit 0
34	PRTADR1	I	1.2V LVCMOS	MDIO Physical Port address bit 1
35	PRTADR2	I	1.2V LVCMOS	MDIO Physical Port address bit 2
36	NC			
37	MSA_BER_Threshold	O	3.3V LVCMOS	BER Threshold signal alarm;
38	NC			
39	3.3V_GND	PWR_GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
40	3.3V_GND	PWR_GND	Ground	
41	3.3V	PWR	Power	3.3V power supply input
42	3.3V	PWR	Power	
43	3.3V	PWR	Power	
44	3.3V	PWR	Power	
45	3.3V_GND	PWR_GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
46	3.3V_GND	PWR_GND	Ground	
47	OHIO_REFCLKn	I	CML	

48	OHIO_REFCLKp	I	CML	OHIO reference clock: Interface is AC coupled, biased, and terminated internal to module. If not using OHIO interface leave unconnected.
49	GND	GND	Ground	Module Ground. Logic and power return path
50	NC			
51	NC			
52	GND	GND	Ground	Module Ground. Logic and power return path
53	GND	GND	Ground	Module Ground. Logic and power return path
54	RX7p	O	CML	Host/Client RX Lane 7; Differential signal, internally AC coupled.
55	RX7n	O	CML	
56	GND	GND	Ground	Module Ground. Logic and power return path
57	RX0p	O	CML	Host/Client RX Lane 0; Differential signal, internally AC coupled.
58	RX0n	O	CML	
59	GND	GND	Ground	Module Ground. Logic and power return path
60	RX1p	O	CML	Host/Client RX Lane 1; Differential signal, internally AC coupled.
61	RX1n	O	CML	
62	GND	GND	Ground	Module Ground. Logic and power return path
63	RX6p	O	CML	Host/Client RX Lane 6; Differential signal, internally AC coupled.
64	RX6n	O	CML	
65	GND	GND	Ground	Module Ground. Logic and power return path
66	RX5p	O	CML	Host/Client RX Lane 5; Differential signal, internally AC coupled.
67	RX5n	O	CML	
68	GND	GND	Ground	Module Ground. Logic and power return path
69	RX2p	O	CML	Host/Client RX Lane 2; Differential signal, internally AC coupled.
70	RX2n	O	CML	
71	GND	GND	Ground	Module Ground. Logic and power return path
72	RX3p	O	CML	Host/Client RX Lane 3; Differential signal, internally AC coupled.
73	RX3n	O	CML	
74	GND	GND	Ground	Module Ground. Logic and power return path
75	RX4p	O	CML	Host/Client RX Lane 4; Differential signal, internally AC coupled.
76	RX4n	O	CML	
77	GND	GND	Ground	Module Ground. Logic and power return path
78	(REFCLKp)	N.C.	N.C.	
79	(REFCLKn)	N.C.	N.C.	

80	GND	GND	Ground	Module Ground. Logic and power return path
81	TX7p	I	CML	Host/Client TX Lane 7; Differential signal, internally AC coupled and terminated.
82	TX7n	I	CML	
83	GND	GND	Ground	Module Ground. Logic and power return path
84	TX0p	I	CML	Host/Client TX Lane 0; Differential signal, internally AC coupled and terminated.
85	TX0n	I	CML	
86	GND	GND	Ground	Module Ground. Logic and power return path
87	TX1p	I	CML	Host/Client TX Lane 1; Differential signal, internally AC coupled and terminated.
88	TX1n	I	CML	
89	GND	GND	Ground	Module Ground. Logic and power return path
90	TX6p	I	CML	Host/Client TX Lane 6; Differential signal, internally AC coupled and terminated.
91	TX6n	I	CML	
92	GND	GND	Ground	Module Ground. Logic and power return path
93	TX5p	I	CML	Host/Client TX Lane 5; Differential signal, internally AC coupled and terminated.
94	TX5n	I	CML	
95	GND	GND	Ground	Module Ground. Logic and power return path
96	TX2p	I	CML	Host/Client TX Lane 2; Differential signal, internally AC coupled and terminated.
97	TX2n	I	CML	
98	GND	GND	Ground	Module Ground. Logic and power return path
99	TX3p	I	CML	Host/Client TX Lane 3; Differential signal, internally AC coupled and terminated.
100	TX3n	I	CML	
101	GND	GND	Ground	Module Ground. Logic and power return path
102	TX4p	I	CML	Host/Client TX Lane 4; Differential signal, internally AC coupled and terminated.
103	TX4n	I	CML	
104	GND	GND	Ground	Module Ground. Logic and power return path

Management interfaces

The protocol for the MSA Management Interface is IEEE 802.3 Clause 45 using the MDIO bus structure with the following additional MDIO interface specifications:

1) Support of MDC rate up to 4 MHz while maintaining downward compatibility to 100 kHz.

2) Both read and write activities occur on the rising edge of MDC clock only;

3) Supports only one MDIO device address.

Table 6 Timing parameters for Host signals

Parameter	Conditions	Min	Typ	Max	Unit
MDIO clock period	Time interval between two consecutive raising or falling MDC edge	250			ns
Host MDIO set-up time	Time interval for which Host MDIO signal must be stable prior to the sampling event of the MDC.	10			ns
Host MDIO hold time	Time interval for which the Host MDIO signal must be stable following the sampling event of the MDC	10			ns
MDC to CFP2 MDIO delay	Time delay among MDC falling edge and CFP2 MDIO state change	0		175	ns
MOD_RSTn assert time	Between falling edge of MOD_RSTn and module entering Reset state			5	ms
MOD_RSTn de-assert time	Between falling edge of MOD_RSTn and module entering Reset state			2.5	s
MOD_LOPWR assert time	Between rising edge of MOD_LOPWR and module entering Low-Power state			10	ms
MOD_LOPWR de-assert time	Between falling edge of MOD_LOPWR and exit of the module from High-Power-up state			10	s
TX_DIS assert time	Between rising edge of TX_DIS and fall of lane output power below 10 % of nominal			100	us
TX_DIS de-assert time	Between falling edge of TX_DIS and rise of lane output power above 90 % of nominal			20	ms
RX_LOS assert time	Between RX input power below LOS threshold and RX_LOS assertion			100	us
RX_LOS de-assert time	Between RX input power above LOS threshold and RX_LOS negation			100	us
GLB_ALRM assert delay time	Between occurrence of the FAWS condition and GLB_ALRMn assertion			150	ms
GLB_ALRM de-assert delay time	Between host clear action of FAWS latched registers and GLB_ALRMn negotiation			150	ms
PRG_ALRM assert time	Between occurrence of the triggering condition and alarm assertion			100	us
PRG_ALRM de-assert time	Between end of the triggering condition and alarm negation			100	us
BERT hardware Alarm	Between end of the triggering condition and alarm negation			100	us

High Speed Signals

The Host/Client interface high-speed signaling consists of 8 transmit and 8 receive differential pairs identified as TX[7:0][p,n] and RX[7:0][p,n]. These signals are operated in 56G PAM4 mode or 26G NRZ mode. PAM4 signaling mode allows connection(s) to 1x400G, 2x200G, or 4x100G Host/Client interfaces. NRZ mode allows connection(s) to 2x100G Host/Client.

Table 7 Lane Mapping

SerDes Lanes	400G	200G	100G	
	400GAUI-8 FOIC4.8 OTUC4 (PAM4)	200GAUI-4 FOIC2.4 OTUC2 (PAM4)	CAUI-4 OTLC.4 OTL4.4 (NRZ)	100GAUI-2 OTLC.2 OTL4.2 (PAM4)
	interface - CH[x,y]			
Tx7[p,n];Rx7[p,n]	CH4.1	CH2.2	CH1.2	CH1.4
Tx6[p,n];Rx6[p,n]				
Tx5[p,n];Rx5[p,n]				CH1.3
Tx4[p,n];Rx4[p,n]				
Tx3[p,n];Rx3[p,n]		CH2.1	CH1.1	CH1.2
Tx2[p,n];Rx2[p,n]				
Tx1[p,n];Rx1[p,n]				CH1.1
Tx0[p,n];Rx0[p,n]				

7. EEPROM

The address allocation of module EEPROM should follow the definition of CFP MSA Management Interface Specification Version 2.6 r06a.

Table 8 CFP Module Memory Map

Address	Description	Standard
8000-807F	CFP NVR 1. Basic ID registers.	CFP MSA MIS V2p6r06a
8080-80FF	CFP NVR 2. Extended ID registers.	CFP MSA MIS V2p6r06a
8100-817F	CFP NVR 3. Network lane specific registers.	CFP MSA MIS V2p6r06a
8180-81FF	CFP NVR 4: Checksum of NVR 3 and MSA-100GLH Extended Identifiers	CFP MSA MIS V2p6r06a
8400-847F	Vendor NVR 1. Vendor data registers.	CFP MSA MIS V2p6r06a
8480-84FF	Vendor NVR 2. Vendor data registers.	CFP MSA MIS V2p6r06a
8800-8FFF	User private use	CFP MSA MIS V2p6r06a

9000-903F	Module Control and Status Registers	
9040-91FF	Network Lane Registers	
9200-9A8F	Client Interface Registers	
9AA0-9ABF	Module Internal Status Data Block	
9AC0-9AC2	Debug Registers to Force Setting of FAWS Events	
9B00-9B37	Client Interface x LLDP Registers	
AC00-AFFF	Common Data Block (CDB) for Command Transactions	CFP MSA MIS V2p6r06a
B000-BFFF	Coherent Module Management Interface	OIF-CFP2-DCO-01.0

8. Mechanical Dimensions

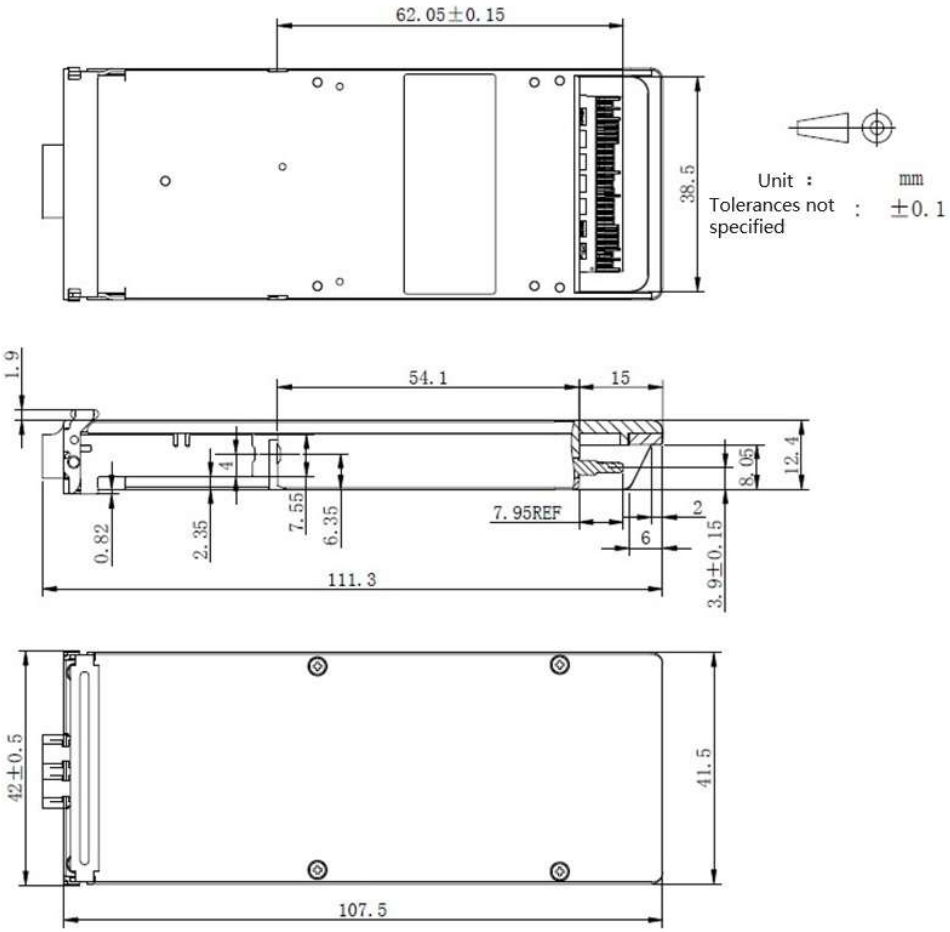

Figure 4 Dimensions

ESD

This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007)

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

9. Module Ordering information

PN	Description
OLQDC41Z	400G CFP2-DCO Module